**Direct Memory Access (DMA)**

**In the Direct Memory Access (DMA) the interface transfer the data into and out of the memory unit through the memory bus. The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of the CPU. Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer. This transfer technique is called Direct Memory Access (DMA).**

**During the DMA transfer, the CPU is idle and has no control of the memory buses. A DMA**

**Controller takes over the buses to manage the transfer directly between the I/O device and**

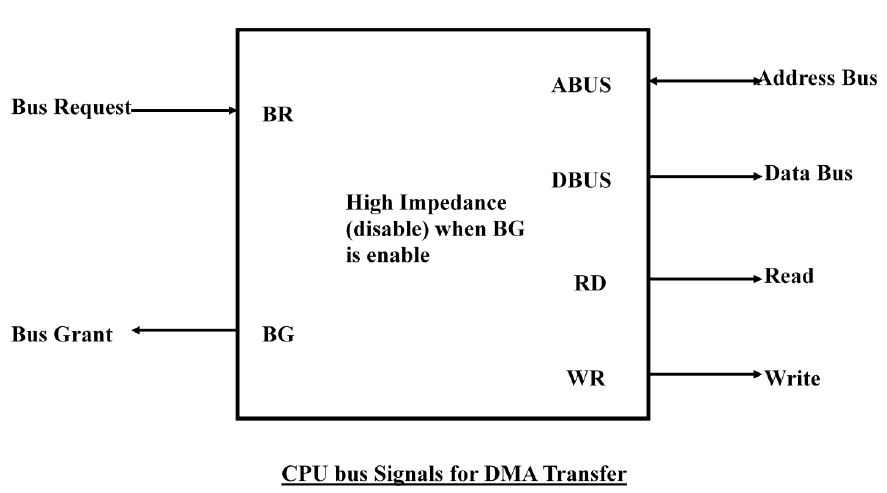
**memory.**

**The CPU may be placed in an idle state in a variety of ways. One common method extensively used in microprocessor is to disable the buses through special control signals**

**such as:**

* **Bus Request (BR)**
* **Bus Grant (BG)**

**These two control signals in the CPU that facilitates the DMA transfer. The Bus Request(*BR)* input is used by the *DMA controller* to request the CPU. When this input is active, the CPU terminates the execution of the current instruction and places the address bus, data bus and read write lines into a *high Impedance state.* High Impedance state means that the output is disconnected.**

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**The CPU activates the Bus Grant (BG) output to inform the external DMA that the Bus Request (BR) can now take control of the buses to conduct memory transfer without processor.**

**When the DMA terminates the transfer, it disables the Bus Request (BR) line. The CPU disables the Bus Grant (BG), takes control of the buses and return to its normal operation.**

**The transfer can be made in several ways that are:**

**1. DMA Burst**

**2. Cycle Stealing**

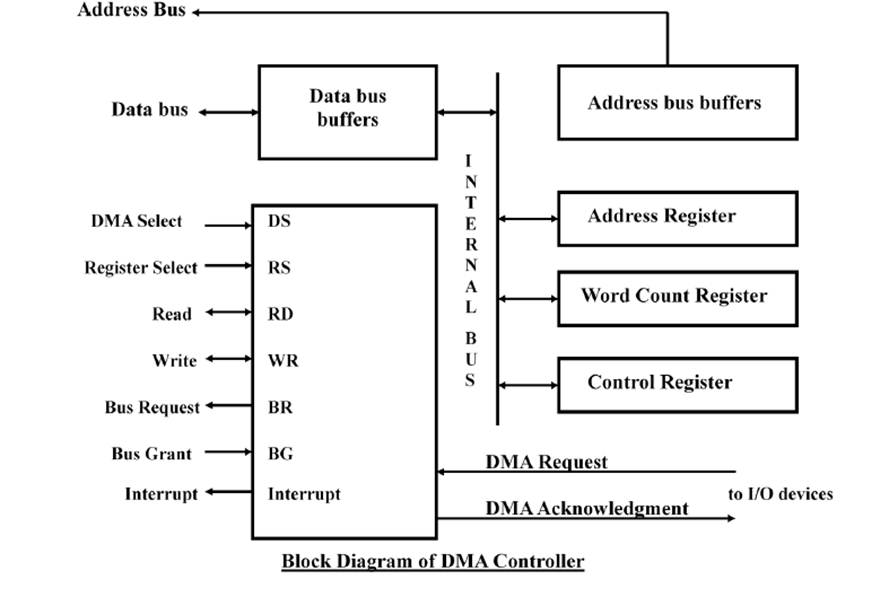
**1 DMA Burst :- In DMA Burst transfer, a block sequence consisting of a number of memory words is transferred in continuous burst while the DMA controller is master of the memory buses.**

**Burst mode is a temporary high-speed data transmission mode used to facilitate sequential data transfer at maximum throughput. Burst mode data transfer rate (DTR) speeds can be approximately two to five times faster than normal transmission protocols.**

**2) Cycle Stealing :- Cycle stealing allows the DMA controller to transfer one data word at a time, after which it must returns control of the buses to the CPU.**

**DMA Controller**

**The DMA controller needs the usual circuits of an interface to communicate with the CPU and I/O device.**

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**The unit communicates with the CPU via the data bus and control lines. The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and RS (Register select) inputs. The RD (read) and WR (write) inputs are bidirectional.**

**When the BG (Bus Grant) input is 0, the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA registers.**

**When BG =1, the DMA can communicate directly with the memory by specifying an address in the address bus and activating the RD or WR control.**

**The DMA controller has three registers:**

**1. Address Register**

**2. Word Count Register**

**3. Control Register**

**1. Address Register: - Address Register contains an address to specify the desired location in memory. The address register is incremented after each word that is transferred to memory.**

**2. Word Count Register: - Word Count Register holds the number of words to be transferred. The register is decremented by one after each word transfer and internally tested for zero.**

**3. Control Register: - Control Register specifies the mode of transfer.**

**Thus the CPU can read from write into the DMA registers under program control via the data bus.**

**The DMA is first initialized by the CPU. After that, the DMA starts and continues to transfer data between memory and peripheral unit until an entire block is transferred.**

**The CPU initializes the DMA by sending the following information through the data bus:**

**1. The starting address of the memory block where data are available (for read) or where data are to be stored (for write)**

**2. The word count, which is the number of words in the memory block**

**3. Control to specify the mode of transfer such as read or write**

**4. A control to start the DMA transfer**

**The starting address is stored in the address register. The word count is stored in the word count register, and the control information in the control register. Once the DMA is initialized, the CPU stops communicating with the DMA unless it receives an interrupt signal or if it wants to check how many words have been transferred.**